AMENDED CLAIMS
[received by the International Bureau on 15 April 2005 (15.04.05);
original claims 1-49 replaced by new claims 1-51 (7 pages)]

1. An information storage process, including:
applying pressure to one or more regions of a substance; and
storing information in said one or more regions by removing said pressure.

2. A process as claimed in claim 1, wherein said one or more regions provide one or more memory cells for a memory device.

3. A process as claimed in claim 2, wherein dimensions of each of said memory cells are on a nanometer scale.

4. A process as claimed in claim 1, including measuring a property of said one or more regions to determine the information stored in said one or more regions.

5. A process as claimed in claim 4, wherein said property includes conductivity or resistance.

6. A process as claimed in claim 1, wherein the applying and removing of pressure includes transforming said one or more regions from at least one first phase to at least one second phase.

7. A process as claimed in claim 6, wherein said at least one first phase includes an amorphous phase, and said at least one second phase includes at least one crystalline phase.

8. A process as claimed in claim 7, wherein said amorphous phase is a relaxed amorphous phase.

9. A process as claimed in claim 8, wherein said substance is substantially silicon.

10. A process as claimed in claim 6, including heating said one or more regions to induce further phase change in said one or more regions.

11. A process as claimed in claim 10, wherein said heating transforms said at least one crystalline phase to a more conductive crystalline phase.

12. A process as claimed in claim 1, wherein the applying and removing of pressure includes controlling at least one of the applying and removing of pressure to determine the information stored in said one or more regions.

13. A process as claimed in claim 1, wherein the step of storing information includes controlling a rate of said removing of said pressure to determine the information stored in said one or more regions.

14. A process as claimed in claim 1, including selecting the pressure applied to each of said one or more regions to determine the information stored in said one or more regions.

15. A process as claimed in claim 14, wherein the pressure is selected from a plurality of predetermined pressures to provide multi-bit information storage in each of said one or more regions.

16. A process as claimed in claim 1, wherein the applying and removing of pressure changes the electrical conductivity of said one or more regions from a first electrical conductivity to a second electrical conductivity, and the process further includes applying pressure to and removing pressure from said one or more regions to change the electrical conductivity of said one or more regions from said second electrical conductivity to a third electrical conductivity.

17. A process as claimed in claim 16, wherein said third electrical conductivity is substantially equal to said first electrical conductivity.

18. A process, including applying pressure to and removing pressure from one or more regions of relaxed amorphous silicon to transform at least a portion of each of said one or more regions into at least one crystalline phase.

19. A process as claimed in claim 18, including the further step of heating said one or more regions to transform the at least one crystalline phase to a further crystalline phase.

20. A process as claimed in claim 19, wherein the further crystalline phase is more electrically conductive than the at least one crystalline phase.

21. A process as claimed in claim 18, including heating said one or more regions to transform the at least one crystalline phase and amorphous silicon in said one or more regions to a further crystalline phase.

22. A process as claimed in claim 18, including controlling the pressure applied to the one or more regions to determine at least one dimension of the at least one crystalline phase in said one or more regions.

23. A process as claimed in claim 22, wherein the pressure applied to each region is selected from a plurality of predetermined pressures.

24. A process as claimed in claim 22, including controlling the further application of pressure to and removal of pressure from said one or more regions to change at least one dimension of the at least one crystalline phase in said one or more regions.

25. A process, including applying pressure to and removing pressure from one or more regions of crystalline silicon in a relaxed amorphous silicon matrix to transform at least a portion of each of said one or more regions into an amorphous phase.

26. A process for producing a structured substance, including:

applying pressure to a plurality of mutually spaced regions of a substance; and

changing at least one material property of said plurality of regions by removing said pressure.

27. A process as claimed in claim 26, wherein said at least one material property includes an electrical property.

28. The process of claim 26, wherein said step of changing includes controlling the removal of said pressure to determine the change in the at least one material property.

29. A process for producing a structured substance, including:

applying pressure to a plurality of mutually spaced regions of a substance; and

inducing a phase change in at least a portion of each of said plurality of mutually spaced regions by removing said pressure.

30. The process of claim 29, wherein the step of inducing a phase change includes controlling the removal of said pressure to determine said phase change.

31. The process of claim 29, wherein the substance is silicon.

32. A process as claimed in claim 29, including heating said one or more regions to induce further phase change in said one or more regions.

33. The present invention also provides a device having components for executing the steps of any one of claims 1 to 32.

34. The present invention also provides a structure produced by executing the steps of any one of claims 1 to 32.

35. A memory device, including a plurality of memory cells created by applying pressure to respective regions of a substance and changing the electrical conductivity of said regions by removing said pressure from said regions to provide said plurality of memory cells.

36. A memory device as claimed in claim 35, wherein dimensions of said memory cells are on a nanometer scale.

37. A memory device, including a plurality of memory cells comprising substantially conducting regions of crystalline silicon in a layer of substantially insulating relaxed amorphous silicon.

38. A memory device, including at least one transforming probe for applying pressure to and removing pressure from selected regions of a substance to store information in the selected regions, the memory device being adapted to control the removing of said pressure to determine the information stored in the selected regions.

39. The memory device of claim 38, wherein the device is adapted to control the applying and the removal of said pressure to determine the information stored in the selected regions.

40. The memory device of claim 38, wherein the device is adapted to repeatedly apply pressure to and remove pressure from selected ones of said regions to modify or erase the information stored in the selected ones of said regions.

41. The memory device of claim 38, wherein the substance is initially one of crystalline silicon and relaxed amorphous silicon.

42. The memory device of claim 38, wherein the applying and removing of said pressure causes a phase change of said substance.

43. A memory device as claimed in claim 38, including at least one electrically conductive probe for determining the electrical conductivities of selected regions of said substance to determine the information stored in the selected regions.

44. A memory device as claimed in claim 38, wherein at least one of said at least one transforming probe is adapted to determine the conductivities of selected regions of said substance to determine the information stored in the selected regions.

45. A memory device as claimed in claim 38, whereby the memory device is adapted to control the removal of pressure from selected ones of said regions to determine the electrical conductivity of the selected regions and thereby the information stored in said regions.

46. A memory device as claimed in claim 39, including a movable support for translating said at least one electrically conductive probe to access selected regions of said device.

47. A memory device as claimed in claim 38, including a movable support for translating said at least one transforming probe to access said selected regions.

48. A memory device, including a plurality of first regions having a first electrical conductivity as a result of applying pressure to and removing pressure from said first regions, a plurality of second regions having a second electrical conductivity, conductive wordlines adjacent said first regions and said second regions, and conductive bitlines adjacent said first regions and said second regions; wherein the conductivity of a selected one of said first regions and said second regions can be determined by accessing a corresponding wordline and a corresponding bitline.

49. A memory device, including a plurality of substantially insulating regions of amorphous silicon in a layer of conducting crystalline silicon, said regions of amorphous silicon formed by applying pressure to and removing pressure from corresponding regions of said layer of conducting crystalline silicon.

50. A memory device, including at least one indenter tip for storing and/or erasing information in cells of said device by indentation of a storage medium to produce phase changes in said storage medium.

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51. A structured material, including one or more substantially crystalline regions in a layer of relaxed amorphous silicon.

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